- **Organization . . . 1 048 576 × 36**
- **Single 5-V Power Supply**
- **72-pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Eight 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Four 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines, in Four Blocks**
- **Separate $\overline{RAS}$ Control for Eighteen Data-In and Data-Out Lines, in Two Blocks**
- **Performance Ranges:**

	ACCESS TIME t_{RAC}	ACCESS TIME t_{CAC}	ACCESS TIME t_{AA}	READ OR WRITE CYCLE	VCC TOLERANCE
'124MBK36-6	60 ns	15 ns	30 ns	110 ns	± 5%
'124MBK36-70	70 ns	18 ns	35 ns	130 ns	± 10%
'124MBK36-80	80 ns	20 ns	40 ns	150 ns	± 10%

- **Operating Free-Air Temperature Range . . . 0°C to 70°C**
- **Presence Detect**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **Long Refresh Period 16 ms (1024 Cycles)**
- **Low Power Dissipation**
- **3-State Output**
- **Gold-Tabbed Version Available:† TM124MBK36**
- **Tin-Lead (Solder) Tabbed Version Available: TM124MBK36Q**

description

The TM124MBK36 is a dynamic random-access memory organized as four times 1 048 576 × 9 (bit 9 is generally used for parity) in a 72 pin leadless single in-line memory module (SIMM). The SIMM is composed of eight TMS44400DJ, 1 048 576 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and four TMS4C1024DJ, 1 048 576 × 1-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs) mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS4C1024DJ is described in the TMS44400 and TMS4C1024 data sheets, respectively.

The TM124MBK36 is available in a double-sided BK leadless module for use with sockets.

The TM124MBK36 features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C

operation

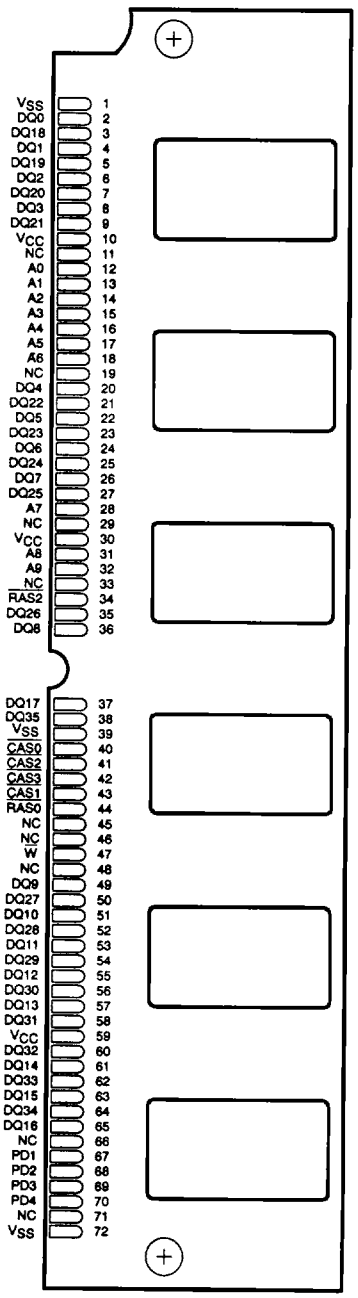
The TM124MBK36 operates as eight TMS44400DJs and four TMS4C1024DJs connected as shown in the functional block diagram and Table 1. Refer to the TMS44400 and TMS4C1024 data sheets for details of operation. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

refresh

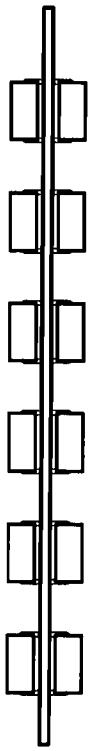
Refresh period is extended to 16 milliseconds and, during this period, each of the 1024 rows must be strobed with $\overline{RAS}$ in order to retain data. Address line A9 must be used as most significant refresh address line (lowest frequency) to assure correct refresh for both TMS44400 and TMS4C1024. A0–A8 address lines must be refreshed every 8 ms as required by the TMS4C1024 DRAM. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

BK SINGLE IN-LINE MODULE†
(TOP VIEW)



TM124MBK36†
(SIDE VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1–PD4	Presence Detects
$\overline{RAS0}$, $\overline{RAS2}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL PIN		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124MBK36	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC

† The package shown here is for pinout reference only and is not drawn to scale.

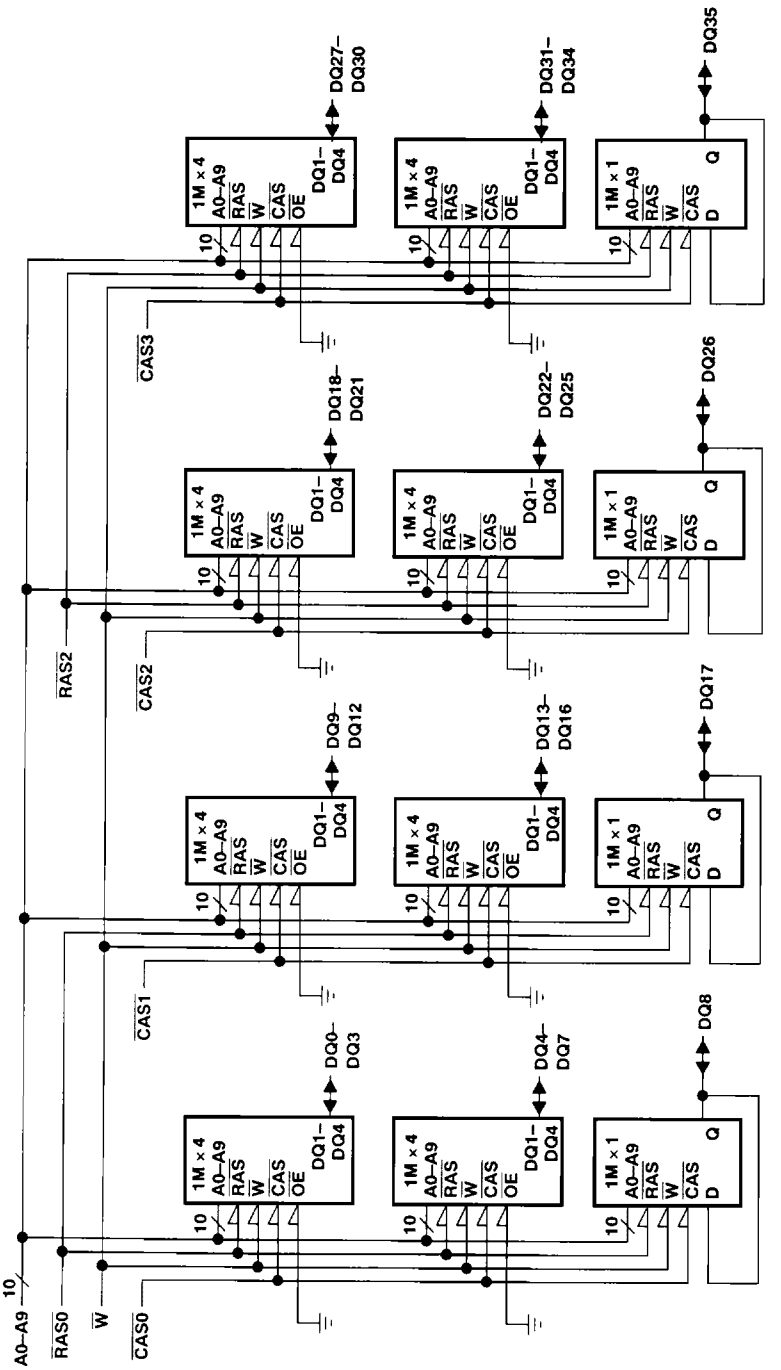
Table 1. Connection Table

DATA BLOCK	$\overline{RAS}x$	$\overline{CAS}x$
DQ–DQ7 DQ8	$\overline{RAS0}$	$\overline{CAS0}$
DQ9–DQ16 DQ17	$\overline{RAS0}$	$\overline{CAS1}$
DQ18–DQ25 DQ26	$\overline{RAS2}$	$\overline{CAS2}$
DQ27–DQ34 DQ35	$\overline{RAS2}$	$\overline{CAS3}$

single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124MBK36: Nickel plate and gold plate over copper.
Contact area for TM124MBK36Q: Nickel plate and tin-lead over copper.

functional block diagram (TM124MBK36)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 12 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM124MBK36-6)	4.75	5	5.25	V
V_{CC}	Supply voltage (TM124MBK36-70/-80)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124MBK36-6		'124MBK36-70		'124MBK36-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		1220		1040		940	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		24		24		24	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		12		12		12	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1200		1040		920	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		1000		880		760	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER			MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs				60	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs				19	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs				38	pF
$C_{i(W)}$	Input capacitance, write-enable input				76	pF
$C_{o(DQ)}$	Output capacitance	DQ8, DQ17, DQ26, DQ35			7	pF
		All other DQ pins			12	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124MBK36-6		'124MBK36-70		'124MBK36-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124MBK36-6		'124MBK36-70		'124MBK36-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time (see Note 9)	10		10		10		ns

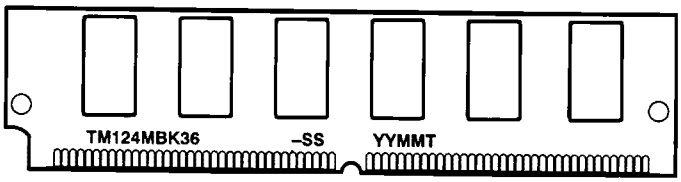
NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'124MBK36-6		'124MBK36-70		'124MBK36-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{DH}	Data hold time	10		15		15		ns
t_{AR}	Column-address hold time after RAS low (see Note 10)	50		55		60		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		12		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 11)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 11)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Write hold time after RAS low	50		55		60		ns
t_{WHR}	$\overline{W}$-high hold time (see Note 9)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 9)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 9)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 12)	15	30	15	35	17	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 12)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 9)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	3	50	3	50	3	50	ns

NOTES: 9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
10. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. The maximum value is specified only to assure access time.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
– SS = Speed Code

NOTE: Location of symbolization may vary.

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