This Data Sheet is Applicable to All TM024EAD9s Manufactured With TMS4C1024s Symbolized With Revision "D" and Subsequent Revisions.

- **TM024EAD9 . . . 1 048 576 × 9 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **30-pin Single-In-Line Package (SIP)**
  – Leadless Module for Use with Sockets
- **Utilizes Nine 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period . . . 8 ms (512 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Performance of Unmounted RAMs:**

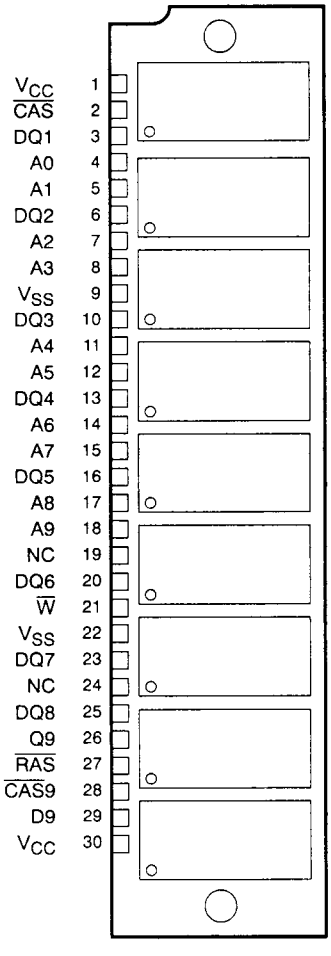
	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)	V_{CC} TOLERANCE
TMS4C1024-6	60 ns	15 ns	110 ns	5%
TMS4C1024-70	70 ns	18 ns	130 ns	10%
TMS4C1024-80	80 ns	20 ns	150 ns	10%
TMS4C1024-10	100 ns	25 ns	180 ns	10%

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free Air Temperature . . . 0°C to 70°C**

description

The TM024EAD9 is a 9216K (dynamic) random-access memory module, organized as 1 048 576 × 9 bits [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS9}$] in a 30-pin single-in-line (SIP) Package.

AD Single-In-Line Package
(Top View)



PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
D9	Data In
NC	No Internal Connection
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

The TM024EAD9 is composed of nine TMS4C1024DJ, 1 048 576 × 1-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate together with decoupling capacitors.

The TMS4C1024DJ is described in the TMS4C1024 data sheet and is fully electrically tested and processed according to TI MIL-STD-883B flows (as ammended for commercial applications) prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

The TM024EAD9 SIP is available in the AD single-sided, leadless module for use with sockets.

The TM024EAD9 SIP is rated for operation from 0°C to 70°C.

operation

The TM024EAD9 operates as nine TMS4C1024DJs shown in the functional block diagram. Refer to the TMS4C1024 data sheet for details of its operation. The common I/O feature of the TM024EAD9 dictates the use of early write cycles to prevent contention on D and Q.

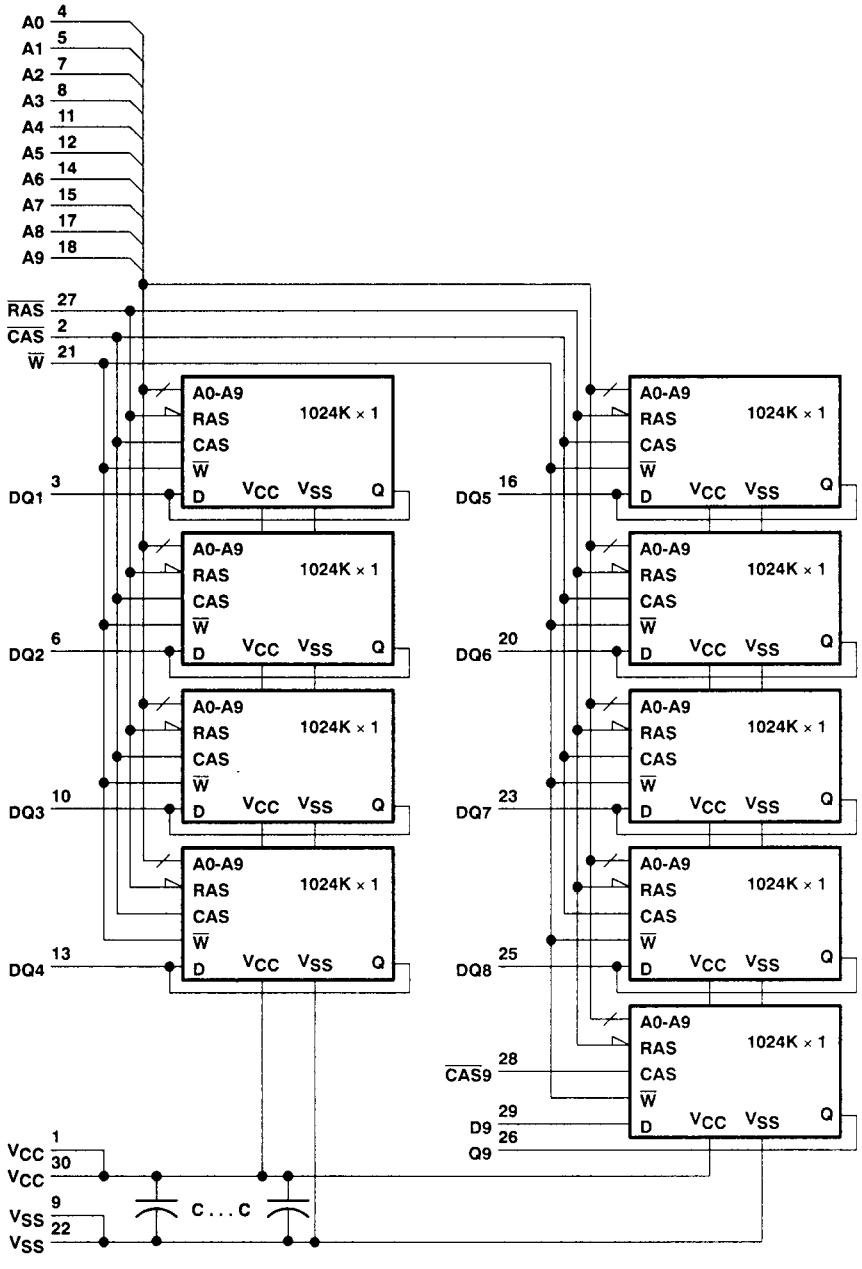
specifications

For TMS4C1024DJ electrical specifications, refer to the TMS4C1024 data sheet.

single-in-line package and components

PC substrate: 1,27 (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate (or coat) on top of copper

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation: ..... 9 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM024EAD9-6)	4.75	5	5.25	V
V_{CC}	Supply voltage (TM024EAD9-70/-80/-10)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM024EAD9-6		TM024EAD9-70		TM024EAD9-80		TM024EAD9-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 to V_{CC}		±10		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	µA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		855		720		675		585	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		18		18		18		18	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		810		720		630		540	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		630		540		450		405	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		45	pF
$C_{i(D)}$	Input capacitance, data input (D9 only)		5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		45	pF
$C_{i(W)}$	Input capacitance, write-enable input		45	pF
$C_{o(DQ)}$	Output capacitance (DQ1-DQ8)		10	pF
C_o	Output capacitance (Q9 only)		7	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

TI single-in-line package nomenclature